IN THE CLAIMS:

Please cancel claims 7 and 8. **Please also amend** claims 1 and 19, and add new claims 22-34, as shown in the complete list of claims that is presented below.

1. (currently amended) A serial bus data control device for use with communication equipment to receive ~~two or more~~ packets sent through a serial bus and each ~~being composed of~~ having a header, actual data positioned subsequently to said header and a footer positioned subsequently to said actual data, comprising:

a preprocessing section to recognize ~~each of said two or more~~ packets received through said serial bus and to divide ~~at least~~ said header, actual data and footer contained in each of said recognized packets into ~~two or more~~ pieces of unit length data each having a predetermined data length; and

a storing section, coupled to said preprocessing section, to temporarily ~~store at least~~ said headers, actual data, and footers contained in ~~each of said~~ packets recognized by said preprocessing section, said headers, actual data, and footers of a plurality of packets being stored in said storing section simultaneously;

wherein said preprocessing section is provided with an address control circuit to assign ~~a continued address of~~ addressing in said storing ~~section, at least, to said unit length data constituting said actual data contained in each of said recognized packets composed of said header, said actual data and said footer, and~~ section for said storing headings, actual data, and footer footers,

wherein said storage section is partitioned into a first data area to store the headers and footers of received packets and a second data area to store the actual data in the received packets, aid

wherein the first data area has a first range of consecutive addresses beginning with a first start address for simultaneously storing said headers and footers of more than one packet, and a second range of consecutive time addresses beginning with a second start address for simultaneously storing said actual data of more than one packet simultaneously.

2. (currently amended) The serial bus data control device according to claim 1, wherein said header contained in each of said packets has information about nodes on a sender side and on a receiver side and wherein ~~a length of data~~ each of said header, said actual data and said footer ~~is~~ has an integral ~~multiple of a storing unit in said storing section.~~ number of bytes.

3. (previously presented) A serial bus data control device for use with communication equipment to receive two or more packets sent through a serial bus and each being composed of a header, actual data positioned subsequently to said header and a footer positioned subsequently to said actual data, comprising:

a preprocessing section to recognize each of said two or more packets received through said serial bus and to divide at least said actual data contained in each of said recognized packets into two or more pieces of unit length data each having a predetermined data length; and

a storing section, coupled to said preprocessing section, to temporarily store at least said actual data contained in each of said packets recognized by said preprocessing section;

wherein said preprocessing section is provided with an address control circuit to assign a continued address of said storing section, at least, to said unit length data constituting said actual data contained in each of said recognized packets composed of said header, said actual data and said footer, and

wherein said address control circuit performs addressing to store said header and said footer, in addition to addressing to store said actual data, and comprises an address signal generating section to generate an address signal used to assign an address of said storing section to said header, said actual data and said footer; an increment signal generating section, coupled to said address signal generating section, to generate an increment signal used to sequentially add said address signal generated by said address signal generating section and to feed said generated increment signal to said address signal generating section; and a decrement signal generating section, coupled to said address generating section, to generate a decrement signal used to sequentially subtract said address signal generated by said address signal generating section and to feed said generated decrement signal to said address signal generating section, and

wherein, when an address is assigned to said header, a supply of said increment signal generated by said increment signal generating section and said decrement signal generated by said decrement signal generating section to said address signal generating section is stopped and, when an address is assigned to said unit length data constituting said actual data, said increment signal is fed from said increment signal generating section sequentially to add said address signal and, when an address is assigned to said footer, after said increment signal has been fed from said increment signal generating section to add said address signal for temporarily storing said footer in said storing section, said decrement signal generated by said decrement signal generating section is fed to said address signal generating section to subtract said address signal

to be given to said footer for causing said footer to be overwritten by a header contained in a subsequently receiving packet.

4. (original) The serial bus data control device according to claim 3, wherein said header is composed of two or more pieces of unit length data each having a unit length and wherein, when an address is assigned to each of said unit length data contained in said header, by stopping a supply of said increment signal and said decrement signal to said address signal generating section to sequentially overwrite said unit length data contained in said header, the same address is assigned to said unit length data contained in said header.

5. (original) The serial bus data control device according to claim 3, wherein, when an address is assigned to said unit length data contained in said actual data, a head address signal used to assign an address to unit length data placed in a head position in said two or more pieces of unit length data contained in said actual data matches an address signal for said header.

6. (original) The serial bus data control device according to claim 3, wherein said footer is composed of two or more pieces of unit length data each having a unit length and wherein, after addressing has been performed by said address signal generating section to store each piece of said unit length data contained in said footer in said storing section, subtraction is done to match an address of said unit length data placed in a head position in said footer with that of a unit length data placed in a head position in a header contained in a subsequently receiving packet for causing said footer to be overwritten by said subsequent packet.

Cancel claims 7 and 8.

9. (previously presented) A serial bus data control device for use with communication equipment to receive two or more packets sent through a serial bus and each being composed of a header, actual data positioned subsequently to said header and a footer positioned subsequently to said actual data, comprising:

a preprocessing section to recognize each of said two or more packets received through said serial bus and to divide at least said actual data contained in each of said recognized packets into two or more pieces of unit length data each having a predetermined data length; and

a storing section, coupled to said preprocessing section, to temporarily store at least said actual data contained in each of said packets recognized by said preprocessing section;

wherein said preprocessing section is provided with an address control circuit to assign a continued address of said storing section, at least, to said unit length data constituting said actual data contained in each of said recognized packets composed of said header, said actual data and said footer,

wherein said storing section has a first data area to store said headers and footers contained in two or more packets in a manner so as to be arranged in a continuous state and a second data area to store two or more pieces of actual data contained in said two or more packets in a manner so as to be arranged in a continuous state,

wherein said address control circuit performs addressing to store said header and said footer in addition to said addressing to store said actual data, and comprises a first address signal generating section to generate an address signal for assigning an address of said first data area to said header and said footer; a second address signal generating section to generate an address

signal for assigning an address of said second data area to said unit length data contained in said actual data; an increment instruction signal generating section to generate a first increment instruction signal for sequentially adding said address signals produced by said first address signal generating section and a second increment instruction signal for sequentially adding said address signals produced by said second address signal generating section and to selectively feed said first and second increment instruction signals to said first and second address signal generating sections; and a switching section to operate in accordance with said first and second increment instruction signals to feed selectively said address signals produced by said first and second address generating sections to said storing section, and

wherein said increment instruction signal generating section, when an address is assigned to said header and said footer, sends out said first increment instruction signal to said first address generating section and, when an address is assigned to said actual data, sends out said second increment instruction signal to said second address generating section.

10. (original) The serial bus data control device according to claim 9, wherein said switching section connects said first and second address signal generating sections selectively to said storing section in accordance with said first increment instruction signal fed from said increment instruction signal generating section to feed said address signal to said storing section.

11. (previously presented) The serial bus data control section according to claim 9, wherein said increment instruction signal generating section comprises:

a register to supply a signal expressing a value of said header, said actual data and said footer;

first and second counters to count said value expressed by said signal fed from said register;

a first gate operated in accordance with an output signal from each of said counters to send out said first increment instruction signal at the time of addressing to store said header and said footer; and

a second gate operated in accordance with an output signal from each of said counters to send out said second increment instruction signal at the time of addressing to store said actual data.

12. (previously presented) The serial bus data control device according to claim 11, wherein said second gate, when said first gate receives simultaneously a gate signal from said first counter and a gate signal from said second counter, receives simultaneously a first signal that is complementary to said gate signal from said first counter and a second signal that is complementary to said gate signal from said second counter.

13. (previously presented) The serial bus data control device according to claim 9, wherein each of said areas in said storing section is partitioned to divided sections to correspond to each of said nodes so that each of the packets received from two or more nodes through said serial bus is stored.

14. (previously presented) The serial bus data control device according to claim 13, wherein each of said first and second data areas is composed of a single area.

15. (previously presented) The serial bus data control device according to claim 13, wherein said preprocessing section is provided with a plurality of address control circuits, each corresponding to one of said nodes, and further comprises a node switching section to selectively supply an address signal fed from said address control circuits to said storing section.

16. (previously presented) The serial bus data control section according to claim 15, wherein each of said divided sections in said both data areas of said storing section has a storage capacity that is variable.

17. (original) The serial bus data control section according to claim 16, wherein said storing capacity of each of said divided sections in said both data areas is able to be adjusted depending on a total amount of data of said header and said footer contained in each of two or more packets sent from each of said nodes and on a total amount of data of said actual data contained in each of two or more packets sent from each of said nodes.

18. (previously presented) The serial bus data control section according to claim 16, wherein each of said address control circuits comprises a first address register and a second address register to store an address showing a head portion of each of said divided sections and an address showing a tail portion of each of said divided sections for specifying each of said divided sections in each of said first and second data areas, and wherein both said addresses assigned to said header and said footer to store in said divided section are stored in said first address register and both said addresses assigned to said actual data to store in said divided section are stored in said second address register.

19. (currently amended) A serial data control method for receiving packets sent through a serial bus, each packet having a header, a footer, and actual data, comprising the steps of:

dividing received packets into actual data portions and header and footer portions;

storing the actual data portions in a first region of a buffer ~~memory,~~ memory and storing the header and footer portions in a second region of the buffer memory, the first region having a first address space defined by a plurality of consecutive addresses for storing the header and footer portions of more than one packet simultaneously and the second region having a second address space that does not overlap the first address space and that is defined by a plurality of consecutive addresses for storing the actual data portions of more than one packet simultaneously.

20. (previously presented) The serial data control method of claim 19, wherein the storing step comprises generating control data address signals and generating actual data address signals.

21. (previously presented) The serial data control method of claim 20, wherein the storing step further comprises selectively switching between the control data address signals and the actual data address signals, and conveying the selected address signals to the buffer memory.

22. (new) The serial data control method of claim 19, wherein the first region of the buffer memory stores actual data portions of a plurality of packets simultaneously, and the

second region of the buffer memory stores header and footer portions of said plurality of packets simultaneously.

23. (new) A serial data control method for receiving packets sent through a serial bus, each packet having a header, a footer, and actual data, comprising the steps of:

(a) diving the header, actual data, and footer in the packets received through the serial bus into pieces of unit length data each having a predetermined length; and

(b) temporarily storing the headers, actual data, and footers in a storing section,

wherein step (b) is conducted such that unit length pieces of header data of a given packet are stored at least temporarily in the storing section and then overwritten by the actual data of the given packet.

24. (new) The serial data control method of claim 23, wherein step (b) is further conducted such that the unit length pieces of header data of the given packet are stored at the same address in the storing section, and storage of the actual data of the given packet begins at said same address, so as to overwrite the last unit length piece of header data of the given packet.

25. (new) The serial data control method of claim 23, wherein step (b) is further conducted such that unit length pieces of footer data of the given packet are stored at least temporarily in said storing section, and then overwritten by the header of a packet immediately following the given packet.

26. (new) The serial data control method of claim 23, wherein step (b) is further conducted such that unit length pieces of the actual data of the given packet are stored at consecutive addresses in the storing section, the number of consecutive addresses corresponding to the number of unit length pieces of actual data in the given packet.

27. (new) The serial data control method of claim 23, wherein the unit length pieces are one byte long.

28. (new) The serial data control method of claim 23, wherein the header in each of the packets has information about nodes on a sender side and on a receiver side.

29. (new) A serial bus data control device for use with communication equipment to receive packets sent through a serial bus and each having a header, actual data positioned subsequently to said header, and a footer positioned subsequently to said actual data, comprising:

a preprocessing section to recognize packets received through the serial bus and to divide the header, actual data, and footer in each of the recognized packets into pieces of unit length data each having a predetermined data length; and

a storing section, coupled to the preprocessing section, to temporarily store the headers, actual data, and footers in the packets recognized by the preprocessing section,

wherein the preprocessing section is provided with an address control circuit to assign addresses such that unit length pieces of header data of a given packet are stored at least temporarily in the storing section and then overwritten by the actual data of the given packet.

30. (new) The serial bus data control device according to claim 29, wherein the unit length pieces of header data of the given packet are stored at the same address in the storing section, and storage of the actual data of the given packet begins at said same address, so as to overwrite the last unit length piece of header data of the given packet.

31. (new) The serial bus data control device according to claim 29, wherein unit length pieces of footer data of the given packet are stored at least temporarily in said storing section, and then overwritten y the header of a packet immediately following the given packet.

32. (new) The serial bus data control device according to claim 29, wherein unit length pieces of the actual data of the given packet are stored at consecutive addresses in the storing section, the number of consecutive addresses corresponding to the number of unit length pieces of actual data in the given packet.

33. (new) The serial bus data control device according to claim 29, wherein the unit length pieces are one byte long.

34. (new) The serial bus data control device according to claim 29, wherein the header in each of the packets has information about nodes on a sender side and on a receiver side.